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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): Azadet 14-6

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Application Number	Filed
10/022,659	12/18/01

First Named Inventor: Azadet et al.

Art Unit	Examiner
2631	Juan A. Torres

Applicant requests review of the final rejection in the above-identified application No amendments are being filed with this request

This request is being filed with a notice of appeal

The review is requested for the reason(s) stated on the attached sheet(s)
Note: No more than five (5) pages may be provided

I am the

- ☐ applicant/inventor
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3 73(b) is enclosed (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 36,597
- ☐ attorney or agent acting under 37 CFR 1 34. Registration number if acting under 37 CFR 1 34 _____

Kevin M. Mason
Signature

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June 4, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required Submit multiple forms if more than one signature is required, see below*.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Azadet et al.
Case: 14-6
Serial No.: 10/022,659
Filing Date: December 18, 2001
Group: 2631
Examiner: Juan A. Torres

Title: Method and Apparatus for Joint Equalization and Decoding of Multilevel Codes

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MEMORANDUM IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The present invention and prior art have been summarized in Applicants' prior responses.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-2, 7-10, 12 and 15-29 are presently pending in the above-identified patent application. Claims 16-19 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan (United States Patent No. 6,418,172) in view of Trans (United States Patent No. 6,377,640). Claims 1, 7, 8, 12, and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of "A Low Complexity Joint Equalizer and Decoder for 1000 Base-T Gigabit Ethernet" (Haratsch 1). Claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Trans, and further in view of Haratsch 1. Claims 2, 9, 10 and 23-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan and Haratsch 1 and further in view of "High Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000Base-T" (Haratsch 2).

Arguments

Claim 16-19

Claims 16-19 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Trans. The Examiner asserts that Raghavan discloses a method for representing an MLT-3 code as a trellis using three signal levels to represent two binary values, the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period; and generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for at least the reason that there exists no motivation to combine the references, and further, even if combinable, the references collectively do not teach each and every limitation of the independent claims. See, e.g., M.P.E.P. §2143.

The Examiner acknowledges that Raghavan does not disclose that a first binary value substantially always causes a *state transition in said trellis* from a first state to a different state and a second binary value does not cause a *state transition in said trellis*," as required by claim 16. The Examiner asserts, however, that this feature is shown by Trans. As previously asserted by Applicants, however, (but **not** addressed by the Examiner at all in the Response to Arguments section of the latest Office Action), Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a trellis). Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a trellis). See, Col. 61, lines 48-56. Trans does not disclose representing an MLT-3 code using a trellis, and thus, states or state transitions are not defined in Trans, as those terms are used by the present invention.

As asserted in Applicants' prior responses, Raghavan discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col. 1, lines 24-36 and FIG. 1A). Thus, in Raghavan (for example, Fig 1A), the input value 1

sometimes causes a transition into the same state, and sometimes a transition into a different state. Thus, one value does not always lead to a state transition as defined in claim 16

Raghavan thus teaches away from using Trans to achieve what is claimed by the present invention, as Raghavan does not define state transitions in the manner required by claim 16 *Compare,* the trellis of Raghavan to the MLT- trellis of the present invention. This "teaching away" is contrary to the combination suggested by the Examiner, even if both references are in the same field of endeavor (Ethernet communications).

Further, even if combinable, the references *collectively* do not teach each and every limitation of the independent claims. As indicated above, Trans does not disclose representing an MLT-3 code using a trellis, and thus, states or state transitions are not defined in Trans, as those terms are used by the present invention. Rather, Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a *trellis*) Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a *trellis*). See, Col 61, lines 48-56.

Thus, Raghaven and Trans, alone or in combination, do not disclose or suggest "generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value *substantially always* causes a state transition in said trellis *from a first state to a different state* and a second binary value does not cause a state transition in said trellis," as required by claim 16

Independent Claims 1 and 8

Independent claims 1 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Haratsch 1. Regarding claims 1 and 8, the Examiner asserts that Raghavan discloses MLT-3 encoding. The Examiner acknowledges that Raghavan does not disclose decoding a signal received from a dispersive channel causing intersymbol interference comprising generating at least one trellis representing the code and the dispersive channel; and performing joint equalization and decoding of the received signal using the trellis. The Examiner asserts, however, that this feature is shown by Haratsch 1.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness, for at least the reason that there exists no motivation to combine the references. See, e.g., M.P.E.P. §2143. First, as asserted in Applicants' prior responses, MLT-3 codes are not trellis coded modulation (TCM) as described by Haratsch 1. Thus, it would not be obvious to a person of ordinary skill in the art to generate a trellis representing the MLT-3 and dispersive channel, in the manner suggested by the present invention.

Furthermore, Haratsch 1 is addressing *four dimensional* TCM codes with 8 states. Thus, the corresponding computations disclosed by Haratsch 1, such as the branch metric computations, do not make sense in the context of the present invention. For example, Equations 1 and 2 of Haratsch 1 do not make sense for MLT-3 codes, as they show the computation of the 1D ISI estimates and 1D branch metrics for each of the 4 dimensions. Page 466, left column, then shows how to combine the 1D branch metric to obtain 4D branch metrics for the 4D TCM code, which again does not make sense for MLT-3 codes. See also Figures 2 and 4, where one and four dimensional branch metric units are shown.

In addition, as discussed hereinafter, if the combination was attempted in the manner suggested by the Examiner, an expression is obtained for the number of states that does not make sense. The number of trellis states in Haratsch 1 is equal to the number of TCM code states and therefore equal to 8. In the present invention, on the other hand, the number of trellis states is $4x(2^K)$, where K is the truncated channel memory.

These incompatibilities between the combination of Raghavan/Haratsch 1 is contrary to the combination suggested by the Examiner, even if both cited references are in the same field of endeavor (Ethernet communications). Thus, a person of ordinary skill in the art would not make such a combination.

In addition to providing a different number of states, which suggests away from the combination, the minimum number of states associated with the present invention ($4x(2^K)=4$ for K=0) is lower than Haratsch 1. This is a "*surprising result*" which is further evidence of non-obviousness. This was **not** addressed by the Examiner in the Response to Arguments section of the latest Office Action.

Furthermore, the Examiner asserts that the motivation for combining Raghavan with Haratsch 1 would be to reduce the complexity of the system. Rather, claims 1 and 8 in fact

generally increase the complexity of the system (joint equalization and decoding using a trellis representing both the MLT-3 code and dispersive channel) compared to a prior art system with a MLT-3 decoder and separate equalizer.

Dependent Claims

Claims 2, 7, 9-10, 12, 15 and 17-29 are dependent on claims 1, 8, or 16, and are therefore patentably distinguished over Raghavan, Haratsch 1 and Haratsch 2 (alone or in any combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

With respect to claims 26 and 29, for example, the Examiner asserts that Haratsch 2 discloses that the number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory (citing page 171). In the passage of Haratsch 2 recited by the Examiner, however, the number of states is given by $Sx(2^{mL})$, where S is the number of TCM code states, m the number of bits that are fed into the TCM encoder, and L is the (full) channel memory. m is defined in Fig.2 of Haratsch 2 for TCM codes, but is undefined for MLT-3 codes, which are different from TCM codes. Significantly, the equation in page 171 of Haratsch 2 uses the channel memory L, while claims 26 and 29 use the truncated channel memory K. Therefore, the equation in page 171 of Haratsch 2 is different and undefined for MLT-3 codes. This was **not** addressed by the Examiner in the Response to Arguments section of the latest Office Action.

Conclusion

All of the pending claims, i.e., claims 1, 2, 7-10, 12 and 15-29, are in condition for allowance and such favorable action is earnestly solicited. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below. The attention of the Examiner and the Pre-Appeal Board to this matter is appreciated.

Respectfully submitted,

Date: June 4, 2007

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